Negative-resistance generator has controllable response

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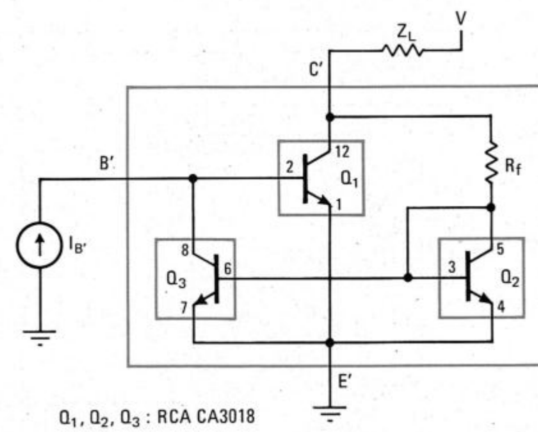
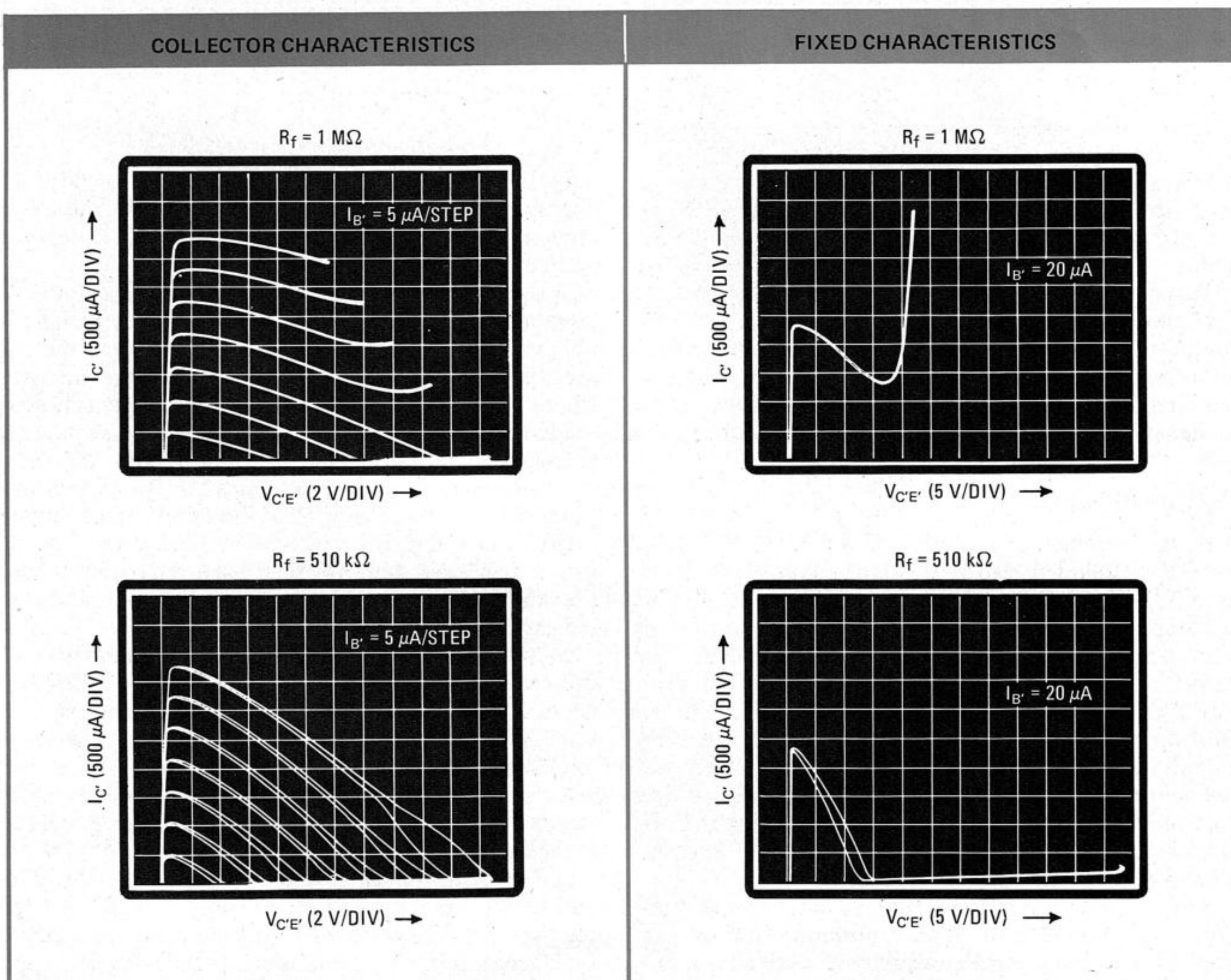
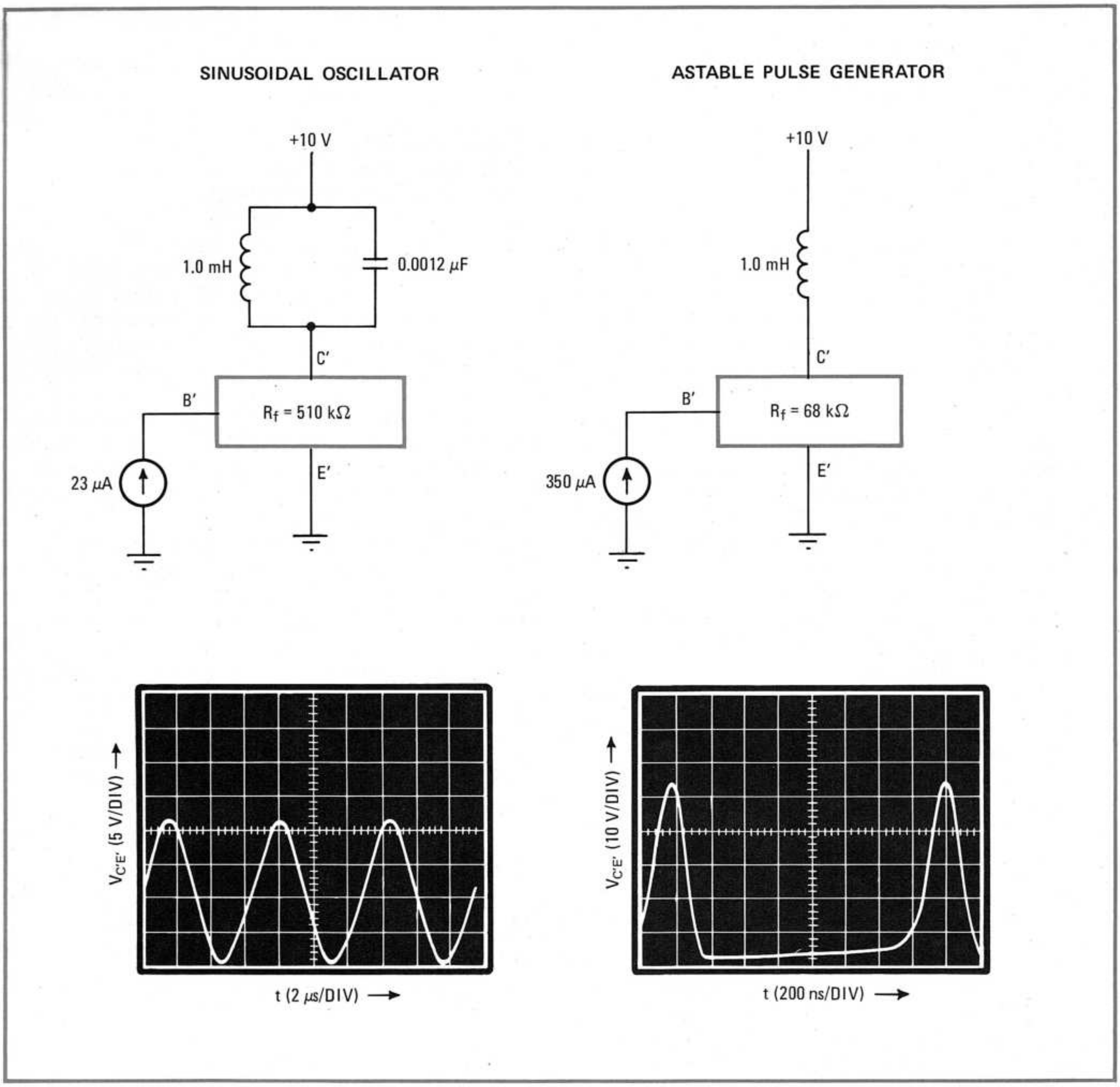
A negative-resistance generator, consisting of three matched transistors, has a current-voltage characteristic that varies with feedback resistance, but not with frequency. When driven by a current source and loaded by an LC resonant circuit, the generator can be operated as a self-starting sinusoidal oscillator. It also can be used for monostable, bistable, or astable pulse generation, as well as oscillator stabilization and switching networks.

The maximum collector current of transistor Q_1 depends on the amount of bias current available at its base terminal. Feedback resistor R_f, along with transistors Q_2 and Q_3, make up a voltage-to-current converter that decreases the base drive of transistor Q_1 when this



Positively negative. Three matched transistors form negative-resistance generator with stable, predictable operating characteristics. Circuit can be treated as transistor that develops negative impedance at terminal C′. Transistors Q_2 and Q_3 and resistor R_f decrease base current of transistor Q_1 whenever Q_1's collector voltage increases. Circuit makes dependable oscillator or pulse generator.





device's collector voltage is increasing.

The negative resistance appearing at Q_1's collector is present at frequencies from dc to several megahertz. The upper frequency limit is determined by the frequency response of both transistor Q_1 and the voltage-to-current converter.

The generator circuit is effectively a three-terminal transistor (with pins labeled B′, C′, and E′). An input current source provides the base current for transistor Q_1, while resistor R_f determines the amount of current fed back to Q_1's base. Because transistors Q_2 and Q_3 are a matched pair and their bases are connected in common, their collector currents will be nearly equal.

As the base current supplied to transistor Q_1 increases, the voltage drop across load impedance Z_L also increases, lowering the potential at Q_1's collector. This lowered potential decreases the collector current through transistors Q_2 and Q_3. The reduced collector current through transistor Q_3 represents an increased impedance at Q_1's base terminal. (A decrease in Q_1's base current has the opposite effect, since Q_3's collector current will be reduced.)

The circuit's operating characteristics are illustrated by the scope traces showing generator performance for two different values of resistor R_f, and for both a fixed and changing bias current. As can be seen, the negative-resistance slope becomes steeper as the value of R_f decreases, from 1 megohm to 510 kilohms, in this instance.

When the load impedance is a parallel LC tank circuit, the negative resistance generator acts as a sinusoidal oscillator, as shown in the figure. Using only an inductor as the load impedance yields an astable pulse generator, which has an output pulse amplitude that equals the breakdown voltage of the combined transistors between terminals C′ and E′. □

BIBLIOGRAPHY

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Controlled starting conditions overcome timing circuit errors

Timing errors of typical RC clock circuits are overcome by the circuit shown. Due to the starting conditions, the time between the first and second clock pulse in conventional designs is often different from the time between a pair of successive pulses that occur later.

This circuit produces an output pulse when the input pulse is received and simultaneously starts the relaxation oscillator. Since C_t is discharged in the quiescent state, the oscillator starts without bias. This is due to the input command, which causes the unijunction transistor to be held in conduction.

The first pulse in the output is derived directly from the input signal, and succeeding output pulses are generated by the oscillator, the timing of which is controlled by R_t C_t. A timing error can be exhibited at turnoff unless R_1 is very small compared to R_t. If R_1 is essentially zero, turnoff time will be controlled by the input command, which is typically a flip-flop output.

The transistor, a General Electric D13T2 programmable unijunction, is compatible with RTL logic if $V_{cc} = 5$ V.

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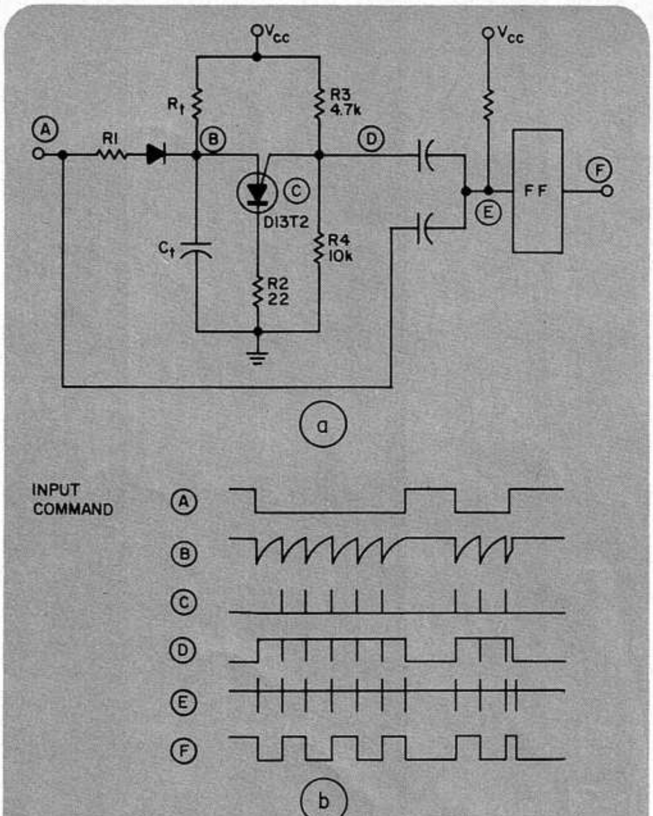

Starting initiated by the input signal is a feature of this timing circuit (a). The waveforms given in "b" correspond to the lettered junctions in "a." Pulse width is determined by R_2C_t.

Negative-resistance circuit is adjustable and versatile

A negative-resistance circuit, which employs only two transistors, offers the advantages of wide dynamic range and easily variable characteristics. Suggested applications for this simple configuration include its use as an oscillator, amplifier, power stabilier, Q multiplier, or an active filter.

The transistors Q_1 and Q_2, type 2SC182 from Nippon, have dc betas of approximately 50—h_{FE1} and h_{FE2}, respectively. The input voltage to the circuit is V, the input current is I, and the supply voltage is V_{CC}.

Neglecting the base-emitter voltages and collector cutoff currents of Q_1 and Q_2, the relationship between I and V is expressed by:

$$I = (h_{FE2}\,V_{CC})/(R_2 + R_3) - [h_{FE1}\,h_{FE2}\,R_2 - (R_2 + R_3)]\,V/[R_1(R_2 + R_3)]$$

Using the circuit parameters shown, this equation can be reduced to:

$$I = (h_{FE2}\,V_{CC}/R_3) - h_{FE1}\,h_{FE2}\,R_2\,V)/R_1\,R_3$$

And finally:

$$I = (25 - 1.25\,V) \times 10^{-3} \text{ amperes}$$

The ideal characteristics of I as a function of V is represented by the solid line in the illustration. However, because the dc beta of real transistors varies with collector current, the actual current-voltage characteristic is shown by the dashed line.

Circuit performance can be easily altered by changing the supply voltage of V_{CC} and the value of the resistors R_1, R_2, R_3 and R_f.

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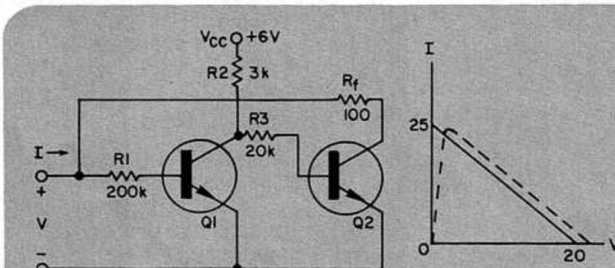

This two-transistor negative-resistance circuit combines simplicity with utility. Its current-voltage characteristic is shown by the dashed line in the graph.

STOP pulse. Meanwhile the cycle counter passes to states 2 through 10.

The next clock puts the cycle counter into state 11, but the gate detects this and clears the BUSY flip-flop. This in turn raises the READY line, resets the cycle counter, and puts the shift register back into the LOAD mode. Thus, the transition from state 10 to the READY mode proceeds asynchronously within a few nanoseconds. During this transition the shift-register output remains high because a logic 1 is loaded from the V_{CC} line.

Transmission at 10 characters per second results if a new character is provided within one clock period (9.09 ms) of this READY indication. Even if a new character is received immediately, however, the output will remain at 1 and transmission will not begin until the next clock. This insures a minimum stop pulse duration of two clock periods. If no character is received, the converter will wait in the READY mode indefinitely.

The following modifications adapt the circuit to the Baudot code. Delete the left-hand 74165, and connect the SI and A inputs of the right-hand 74165 to V_{CC}. Then replace the 7410 gate with a 7404 inverter driven off the 7493's D output (the A output now connects only to B_{in}; B and C outputs are left with no connection). □

Complementary JFETS form bimode oscillator

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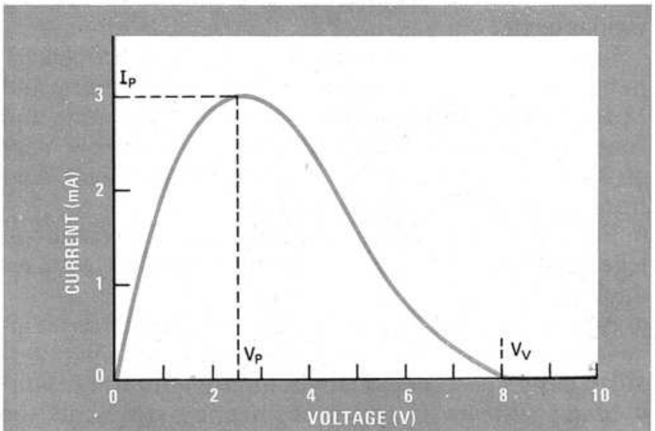
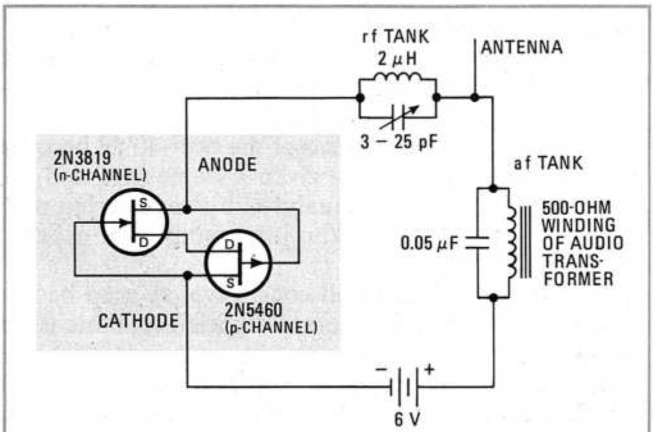
A complementary pair of junction field-effect transistors can be interconnected to form a negative-resistance two-terminal device, which makes a simple oscillator. In monolithic form this configuration is called a lambda diode [*Electronics*, June 26, p. 105] and is available with a wide range of characteristics. If two discrete JFETs are connected to make the diode, they do not have to be matched, but can be chosen to provide various values of peak current and negative-resistance-voltage range. Figure 1 shows current as a function of voltage for a combination consisting of an n-channel 2N3819 and a p-channel 2N5460.

The JFET "diode" can be made to oscillate at frequencies ranging from audio to vhf. All that is required is to connect the diode in series with an inductance-capacitance tank circuit and supply a bias voltage in the negative-resistance region. Figure 2 shows a simple bimode oscillator circuit capable of oscillating at both audio and radio frequencies simultaneously. Oscillation is at approximately the natural resonances of each tank circuit. The radio-frequency tank, consisting of a 2-microhenry choke shunted by a trimmer capacitor, can be tuned over a wide range centered near 20 megahertz. The audio section uses the 500-ohm winding of a miniature audio output transformer and a 0.05-microfarad ceramic capacitor for oscillation at approximately 440 hertz. The audio section cleanly amplitude-modulates the rf section, as demonstrated by reception of the radiated signal on a communications receiver. Power output is in the order of 25 milliwatts and the signal has a range of several hundred feet with no antenna on the oscillator. The range can be extended to several thousand feet with a short length of antenna, so a form of this oscillator can be adapted to radio-control appplications.

This circuit can be used as a simple signal source for many experimental purposes. The audio section can be eliminated or shorted out if an unmodulated signal is desired. The circuit can also be adapted to any design requiring a low-level signal source. Variable frequency control can be incorporated at either or both frequency levels. □



1. Negative resistance. Current-voltage characteristics are shown for a "diode" consisting of the arrangement of the two complementary JFETS shown in Fig. 2. For any terminal voltage between 2.5 V and 8 V, the combination has a negative resistance.



2. Bimode oscillator. JFET-combination "diode" and two tank circuits can oscillate at audio frequency and radio frequency simultaneously. Resultant signal is rf modulated by af; either component can be varied for communications or control applications.